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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Paul Broyles

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HEWLETT PACKARD COMPANY

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INTELLECTUAL PROPERTY ADMINISTRATION

FORT COLLINS, CO 80527-2400

EXAMINER

MANOSKEY, JOSEPH D

ART UNIT

PAPER NUMBER

2113

MAIL DATE

DELIVERY MODE

05/16/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,523	BROYLES, PAUL	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 March 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein et al., U.S. Patent 6,145,102, hereinafter referred to as "Klein", in view of Garnett et al., U.S. Patent 7,124,321, hereinafter referred to as "Garnett".

3. Referring to claim 1, Klein teaches a computer executing a self test of components of the computer which have their status monitored, this is interpreted as a method of verifying compatibility of components in a computer system (See Col. 1, lines 22-30 and Col. 2, lines 54-59). Klein teaches monitoring the power supply with the actual voltage and current levels being reported. Set limits can be monitored and an error message can be transmitted in the event the limits are exceeded (See Col. 3, line 64 to Col. 4, line 5). This is interpreted as, determining a host maximum power value indicating the maximum power the computer system is rated to supply, and if the CPU maximum power value exceeds the host maximum power value, invoking a first error handler.

Klein does not teach reading, from at least one CPU register, a CPU maximum power value indicating the maximum power the CPU is rated to consume during operation, however Klein does teach the power supply monitor having limits sets and determining that these set limits have been exceeded, Klein is silent on how the value of the limits is stored (See Col. 4, lines 1-5). Garnett teaches a environmental monitor that includes limit values stored in limit registers that include values of voltages and temperatures (See Col. 25, lines 4-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the monitoring of limits of values with registers of Garnett with the status monitoring of Klein. This would have been obvious to one ordinary skill in the art at the time of the invention to do because the registers allow for comparisons to be made of the limit values (See Garnett, Col. 25, lines 11-14).

4. Referring to claim 2, Klein and Garnett disclose all the limitations (See rejection of claim 1) including monitoring temperatures in the computer and running a fan faster depending on the reading of the temperature, this is interpreted as reading, from at least one CPU register, a CPU maximum temperature value indicating the maximum temperature at which the CPU is rated to operate, determining a host minimum temperature value indicating the minimum CPU temperature the host is rate to maintain, and if the host minimum temperature value exceeds the CPU maximum temperature value, invoking a second error handler (See Klein, Col. 3, lines 53-57 and Col. 4, lines 32-45).

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5. Referring to claim 3, Klein and Garnett teach all the limitations (See rejection of claim 2) including a transmission of an error message in the event of any computer failure which inactivates various components, this is interpreted as the first and second error handlers are the same error handler (See Klein, Col. 1, lines 39-43).
6. Referring to claim 4, Klein and Garnett disclose all the limitations (See rejection of claim 2) including the computer executing a self-test form the boot ROM at boot up, this is interpreted as the CPU maximum power value and the CPU maximum temperature value are read from the same CPU register (See Klein, Col. 2, lines 54-59).
7. Referring to claim 5, Klein and Garnett teach all the limitations (See rejection of claim 1) including a power supply monitor with limits set therein, this is interpreted as determining the host maximum power value comprises identifying a motherboard and a chassis of the computer system (See Klein, Col. 4, lines 2-5).
8. Referring to claim 6, Klein and Garnett teach all the limitations (See rejection of claim 5) including monitoring the power supply which includes power supply voltages, this is interpreted as identifying the motherboard comprises determining voltage regulation characteristics of the motherboard (See Klein, Col. 3, lines 64-66).

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9. Referring to claim 7, Klein and Garnett disclose all the limitations (See rejection of claim 5) including the computer executing a self-test from the boot ROM at boot up, this is interpreted as identifying the motherboard comprises reading a register on the motherboard (See Klein, Col. 2, lines 54-59).

10. Referring to claim 8, Klein and Garnett teach all the limitations (See rejection of claim 5) including monitoring the power supply and monitoring temperatures in the chassis of the computer, this is interpreted as identifying the chassis comprises determining power supply and cooling characteristics of the chassis (See Klein, Col. 3, lines 47-57).

11. Referring to claim 9, Klein and Garnett disclose all the limitations (See rejection of claim 5) including a chassis intrusion sensor coupled to an interface, this is interpreted as identifying the chassis comprises reading hardwired pins of a chassis connector (See Klein, Col. 58-60).

12. Referring to claim 10, Klein and Garnett teach all the limitations (See rejection of claim 2) including monitoring the power supply and monitoring temperatures in the chassis of the computer, this is interpreted as the host minimum temperature value is determined responsive to cooling characteristics of a chassis of the computer system and to the maximum CPU power value (See Klein, Col. 3, lines 47-57).

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13. Referring to claim 11, Klein and Garnett teach all the limitations (See rejection of claim 1) including that upon failure of the self test the computer presents and error message on a screen, this is interpreted as the first error handler causes an error message to be displayed (See Klein, Col. 2, lines 63-65).

14. Referring to claim 12, Klein and Garnett disclose all the limitations (See rejection of claim 1) including the power supply monitoring can turn off the power, this is interpreted as the first error handler causes the computer system to be powered down (See Klein, Col. 4, lines 41-45).

15. Referring to claim 13, Klein teaches a computer executing a self test of components of the computer which have there status monitored from a boot ROM, this is interpreted as a machine-readable storage or transmission medium containing code that, when executed on a computer system, causes the computer system to perform a method of verifying compatibility of components in a computer system (See Col. 1, lines 22-30 and Col. 2, lines 54-59).

Klein teaches monitoring the power supply with the actual voltage and current levels being reported. Set limits can be monitored and an error message can be transmitted in the event the limits are exceeded (See Col. 3, line 64 to Col. 4, line 5). This is interpreted as determining a host maximum power value indicating the maximum power the computer system is rated to supply, and if the CPU maximum power value exceeds the host maximum power value, invoking a first error handler.

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Klein does not teach reading, from at least one CPU register, a CPU maximum power value indicating the maximum power the CPU is rated to consume during operation, however Klein does teach the power supply monitor having limits sets and determining that these set limits have been exceeded, Klein is silent on how the value of the limits is stored (See Col. 4, lines 1-5). Garnett teaches a environmental monitor that includes limit values stored in limit registers that include values of voltages and temperatures (See Col. 25, lines 4-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the monitoring of limits of values with registers of Garnett with the status monitoring of Klein. This would have been obvious to one ordinary skill in the art at the time of the invention to do because the registers allow for comparisons to be made of the limit values (See Garnett, Col. 25, lines 11-14).

16. Referring to claim 14, Klein and Garnett disclose all the limitations (See rejection of claim 13) including monitoring temperatures in the computer and running a fan faster depending on the reading of the temperature, this is interpreted as reading, from at least one CPU register, a CPU maximum temperature value indicating the maximum temperature at which the CPU is rated to operate, determining a host minimum temperature value indicating the minimum CPU temperature the host is rate to maintain, and if the host minimum temperature value exceeds the CPU maximum temperature value, invoking a second error handler (See Klein, Col. 3, lines 53-57 and Col. 4, lines 32-45).

17. Referring to claim 15, Klein and Garnett teach all the limitations (See rejection of claim 14) including a transmission of an error message in the event of any computer failure which inactivates various components, this is interpreted as the first and second error handlers are the same error handler (See Klein, Col. 1, lines 39-43).

18. Referring to claim 16, Klein and Garnett disclose all the limitations (See rejection of claim 14) including the computer executing a self-test from the boot ROM at boot up, this is interpreted as the CPU maximum power value and the CPU maximum temperature value are read from the same CPU register (See Klein, Col. 2, lines 54-59).

19. Referring to claim 17, Klein and Garnett teach all the limitations (See rejection of claim 13) including a power supply monitor with limits set therein, this is interpreted as determining the host maximum power value comprises identifying a motherboard and a chassis of the computer system (See Klein, Col. 4, lines 2-5).

20. Referring to claim 18, Klein and Garnett teach all the limitations (See rejection of claim 17) including monitoring the power supply which includes power supply voltages, this is interpreted as identifying the motherboard comprises determining voltage regulation characteristics of the motherboard (See Klein, Col. 3, lines 64-66).

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21. Referring to claim 19, Klein and Garnett disclose all the limitations (See rejection of claim 17) including the computer executing a self-test from the boot ROM at boot up, this is interpreted as identifying the motherboard comprises reading a register on the motherboard (See Klein, Col. 2, lines 54-59).

22. Referring to claim 20, Klein and Garnett teach all the limitations (See rejection of claim 17) including monitoring the power supply and monitoring temperatures in the chassis of the computer, this is interpreted as identifying the chassis comprises determining power supply and cooling characteristics of the chassis (See Klein, Col. 3, lines 47-57).

23. Referring to claim 21, Klein and Garnett disclose all the limitations (See rejection of claim 17) including a chassis intrusion sensor coupled to an interface, this is interpreted as identifying the chassis comprises reading hardwired pins of a chassis connector (See Klein, Col. 58-60).

24. Referring to claim 22, Klein and Garnett teach all the limitations (See rejection of claim 14) including monitoring the power supply and monitoring temperatures in the chassis of the computer, this is interpreted as the host minimum temperature value is determined responsive to cooling characteristics of a chassis of the computer system and to the maximum CPU power value (See Klein, Col. 3, lines 47-57).

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25. Referring to claim 23, Klein and Garnett teach all the limitations (See rejection of claim 13) including that upon failure of the self test the computer presents and error message on a screen, this is interpreted as the first error handler causes an error message to be displayed (See Klein, Col. 2, lines 63-65).

26. Referring to claim 24, Klein and Garnett disclose all the limitations (See rejection of claim 13) including the power supply monitoring can turn off the power, this is interpreted as the first error handler causes the computer system to be powered down (See Klein, Col. 4, lines 41-45).

Response to Arguments

27. Applicant's arguments, see page 7 of amendment, filed 25 January 2007, with respect to claims 13-24 have been fully considered and are persuasive. The 35 U.S.C. 101 rejection of claims 13-14 has been withdrawn.

28. Applicant's arguments, see pages 7 and 8 of amendment, filed 25 January 2007, with respect to the rejection(s) of claim(s) 1-24 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of new found prior art, see above rejection.

Conclusion


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29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
May 11, 2007


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